Epitaxial Lift-Off for Vertical GaN Power Devices

Patrick Fay, Jingshan Wang, Lina Cao
Department of Electrical Engineering
University of Notre Dame
Notre Dame, IN 46556
Email: pfay@nd.edu

Robert McCarthy, Rekha Reddy, Chris Youtsey
MicroLink Devices, Inc.
Niles, IL 60714

Jinqiao Xie, Ed Beam
Qorvo, Inc.
Richardson, TX 75080

***Abstract*—Epitaxial lift-off using band gap selective photo-electrochemical etching is demonstrated for vertical GaN power devices. The use of a pseudomorphic InGaN release layer enables low dislocation-density material to be achieved on bulk GaN substrates; this enables high breakdown voltages and low reverse leakage currents to be achieved. Demonstrations of bipolar GaN pn junction diodes show that device electrical performance is not compromised by the lift-off processing. Thermal performance can also be improved by directly bonding the lifted off devices to high-thermal conductivity carriers. Epitaxial liftoff has the potential to improve size, cost, weight, and thermal performance of power electronics, as well as enabling heterogeneous integration.**

Keywords*—*GaN power devices; vertical GaN devices; epitaxial lift-off; fabrication processing

I. Introduction

GaN and related III-N materials are promising for high-efficiency, high-power applications due to the combination of wide band gap and excellent electron transport. While HEMTs dominate RF applications, vertical devices are attractive for power applications because they offer improved scalability for high voltages and high currents and are less sensitive to surface effects. However, the high threading dislocation density that results from growth on non-native substrates can lead to increased leakage current and reduced breakdown [1]. This can be mitigated through the use of native GaN substrates, but these substrates are currently available in small sizes and at high cost. Epitaxial lift-off (ELO) processing with a pseudomorphic release layer provides a route to realize high-performance vertical GaN devices for power applications that reduces device size, weight, and cost by enabling low dislocation density, efficient integration, and substrate re-use, while also improving thermal performance.

II. Device Design and Fabrication

To demonstrate the performance advantages possible with ELO of vertical GaN power devices, vertical pn diodes have been fabricated. A bipolar device was selected for the demonstration to highlight any impact on the material quality caused by the ELO processing, since bipolar devices are very sensitive to defects such as recombination centers; the approach described here has also been analyzed for use with vertical JFETs with similar benefits [2]. Figure 1 shows a

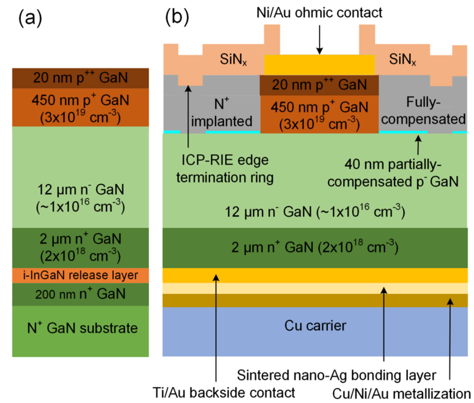

Fig. 1. (a) Device structure for ELO devices; the control devices used the same structure except without the InGaN release layer. (b) Schematic cross-section of the ELO devie after processing. Adapted from [8].

schematic cross-section of the devices; in addition to the structure shown in Fig. 1, devices on identical material except without the release layer have been fabricated for comparison. To facilitate the ELO process using band gap selective photoelectrochemical (PEC) wet etching, a pseudomorphic InGaN release layer is inserted in the device structure below the n+ cathode contact layer. Except for the release layer, the device and fabrication processing is conventional; devices with the same active layer design and edge termination have been reported previously [3]. For the PEC ELO process, the sample is immersed in a KOH solution to form an electrochemical cell; the sample is the anode and a Pt wire serves as the cathode. UV LEDs are used to illuminate the wafer through from the back to drive the electrochemical etching. The peak irradiance of the UV light is at a photon energy below GaN's band gap so that absorption occurs only in the InGaN layer. This allows enables high etch selectivity between the InGaN release layer and the GaN device layers, as needed for effective large-area lift-off. Full details of the ELO process can be found in [4-5]; wafer-scale lift-off as well as die-scale liftoff is possible with this technique, and re-use of the GaN substrate after lift-off has also been demonstrated [6]. After lift-off, the devices were bonded to a copper carrier using nanosilver paste [7] and sintering at 260 °C. This layer transfer and bonding approach is amenable to bonding to heatsinks (as demonstrated here) or for facilitating heterogenous integration.

III. Device Performance

Electrical characterization shows nearly identical performance of control devices and devices that have been lifted off and transferred to a copper carrier. Figure 2(a) shows a comparison of the forward bias characteristics for both ELO and control devices; from the slope of the forward characteristics an ideality factor of 2 is obtained for both device types at low current densities, dropping to approximately 1.5 before the series-resistance roll-over seen in Fig. 2 [8]. The nearly identical ideality factor behavior indicates that the Shockley-Read-Hall recombination in the two device types is the same, suggesting that the ELO processing has not introduced additional defects or recombination centers. The breakdown performance is shown in Fig. 2(b); as can be seen, the devices exhibit nearly identical breakdown voltages of 1.3 kV [7]; ELO processing does not adversely impact the reverse breakdown, despite the ELO processing and bonding to a copper carrier. Current densities over 8 kA/cm^2 have been obtained; under pulsed conditions, devices with 1 mm diameter have been demonstrated with 12 A forward currents [3].

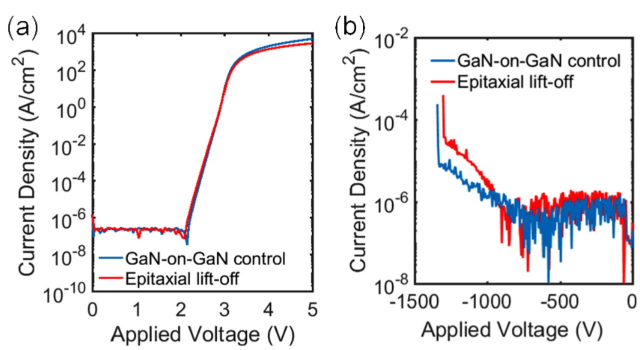

Fig. 2. Comparison of (a) forward bias and (b) reverse bias characteristics of ELO and control devices [8]. Nearly identical performance is obtained.

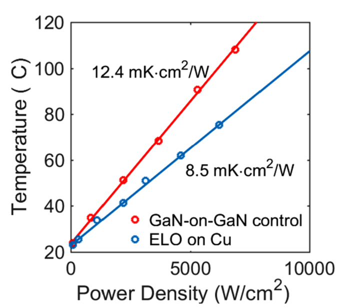

Fig. 3. Temperatue vs. forward-bias power density for GaN-on-GaN control device and ELO device mounted to copper carrier, as determined using forward-bias pulsed I-V characterization. Adapted from [8].

The much thinner device profile after ELO substrate removal (device thickness ~15 µm, vs. ~450 µm for devices on the substrate) also has the potential to improve the thermal performance of the devices. The thermal resistance of the devices with and without ELO processing has been assessed by both pulsed I-V characterization as well as electroluminesence measurements. By using forward-bias pulses to induce self-heating in the devices, the thermal resistance can be extracted as shown in Fig. 3. A thermal resistance of 12.4 mKcm^2/W is extracted for control devices on GaN substrates, vs. 8.5 mKcm^2/W for the ELO devices. Forward-bias electroluminesence measurements (Fig. 4) show a similar thermal resistance; the electroluminesence peak red-shifts with

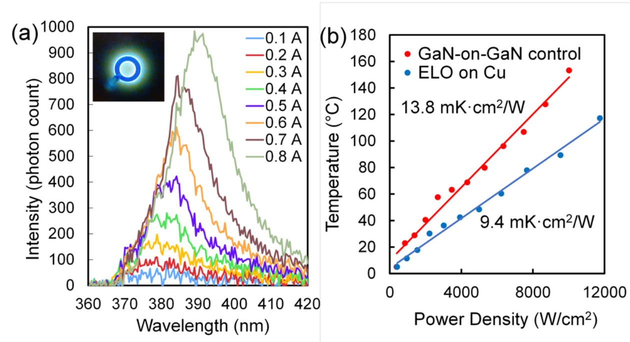

Fig. 4. (a) Electroluminescence intensity vs. wavelength an ELO device (160 μm diameter) vs. bias. (b) Device temperature inferred from the peak of the electroluminescence vs. applied power for control and ELO devices. Adapted from [8].

increasing current drive due to self-heating; from the band gap's depdence on temperature the thermal resistnace can be extracted. As shown in Fig. 4, similar thermal resistances (13.8 mKcm^2/W for the control, 9.4 mKcm^2/W for the ELO device) are obtained.

IV. Conclusions

Epitaxial lift-off using band gap selective PEC etching from a pseudomorphic InGaN release layer allows the fabrication of vertical GaN power devices with excellent electrical and thermal performance. The epitaxial lift-off approach demonstrated here enables use of low-dislocation density material to achieve devices with low leakage and high breakdown, while simultaneously reducing size, weight, and cost and improving device thermal resistance for improved power handling capability. Bipolar pn junctions were selected for the demonstration reported here due to their sensitivity to defect formation; the results show that no additional recombination centers or other defects that compromise device performance are generated by the ELO processing. The PEC ELO technique is also promising for other vertical GaN devices, such as vertical MOSFETs or JFETs. The epitaxial lift-off and transfer process demonstrated here also provides an promising approach to heterogeneous integration of III-N devices with other materials and substrates for system-in-package and system-on-chip applications.

Acknowledgment

This work was supported in part by the ARPA-E SWITCHES program.

References

[1] E. Miller, E. Yu, P. Waltereit, and J. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Appl. Phys. Lett.* vol. 84, pp. 535-537, Jan. 2004

[2] J. Wang "High Power Vertical GaN Electronic Devices Formed by Epitaxial Liftoff," PhD. Dissertation, Univ. of Notre Dame, 2018.

[3] J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, and P. Fay, "High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination," *Appl. Phys. Lett.* vol. 113(2), Jul. 2018.

[4] C. Youtsey, R. McCarthy, R. Reddy, K. Forghani, A. Xie, E. Beam, J. Wang, P. Fay, T. Ciarkowski, E. Carlson, and L. Guido, "Wafer-scale epitaxial lift-off of GaN using bandgap-selective photoenhanced wet etching," *Physica Status Solidi (b)*, vol. 254, p. 1600774, Aug. 2017.

[5] C. Youtsey, R. McCarthy, R. Reddy, A.y Xie, E. Beam, J. Wang, P. Fay, E. Carlson, and L. Guido, “Epitaxial Lift-Off from Native GaN Substrates Using Photoenhanced Wet Etching,” in *CS MANTECH*, 2017, vol. 16.5, pp. 1-4.

[6] H. Amano, et al., “The 2018 GaN power electronics roadmap,” *J. of Physics D: Appl. Physics,* vol. 51, p. 163001, Mar. 2018.

[7] Y. Tan, X. Li, X. Chen, G. Lu, and Y. Mei, “Low-Pressure-Assisted Large-Area (> 800 mm 2) Sintered-Silver Bonding for High-Power Electronic Packaging,” *IEEE Trans. on Components, Packaging and Manufacturing Tech.*, vol. 8, pp.202-209, Feb. 2018.

[8] J. Wang, R. McCarthy, C. Youtsey, R. Reddy, J. Xie, E. Beam, L. Guido, L. Cao, and P. Fay, “High Voltage Vertical GaN p-n Diodes by Epitaxial Lift-Off from Bulk GaN Substrates,” *IEEE Electron Dev. Lett.,* in press, 2018.